# VISIBL SEMICONDUCTORS™

YC Demo Day Pitch

https://youtu.be/kVVK7uUB3bo

Jordon Kashanchi

Microsoft (Azure Maia 100, 200, X00), Intel, Arm, MS ECE, UT Austin — published in PNAS & ACM

Bryce Neil

Deloitte OmniaAI - Recipient of two of Canada's three nomination-based top academic scholarships — BASc. Computer Engineering

$1.6 Trillion

---

Custom ASICs for 6 customers

$1.6 Trillion ← Broadcom

---

Custom ASICs for 6 customers

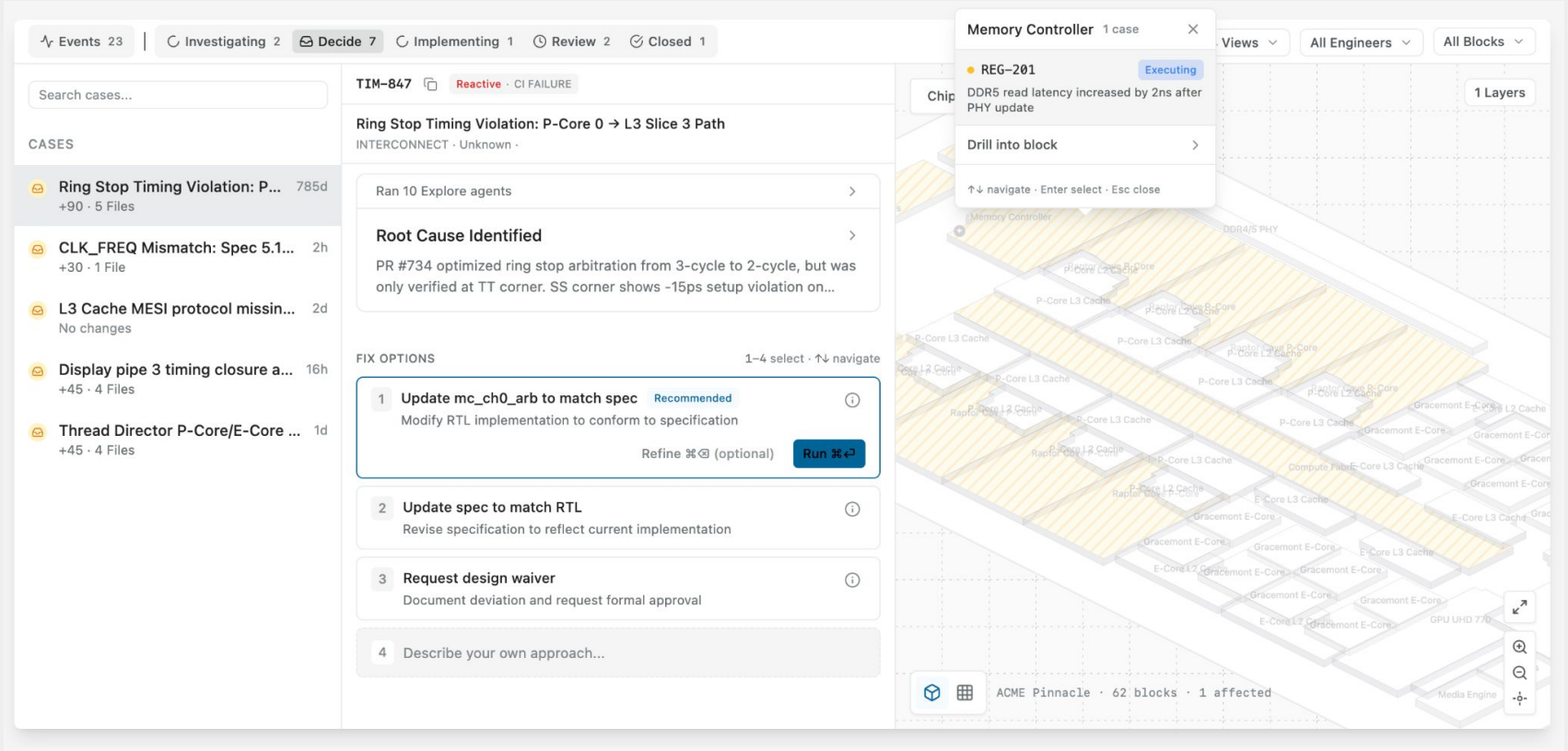
$1.6 Trillion + 1 Trillion (Shadow market)

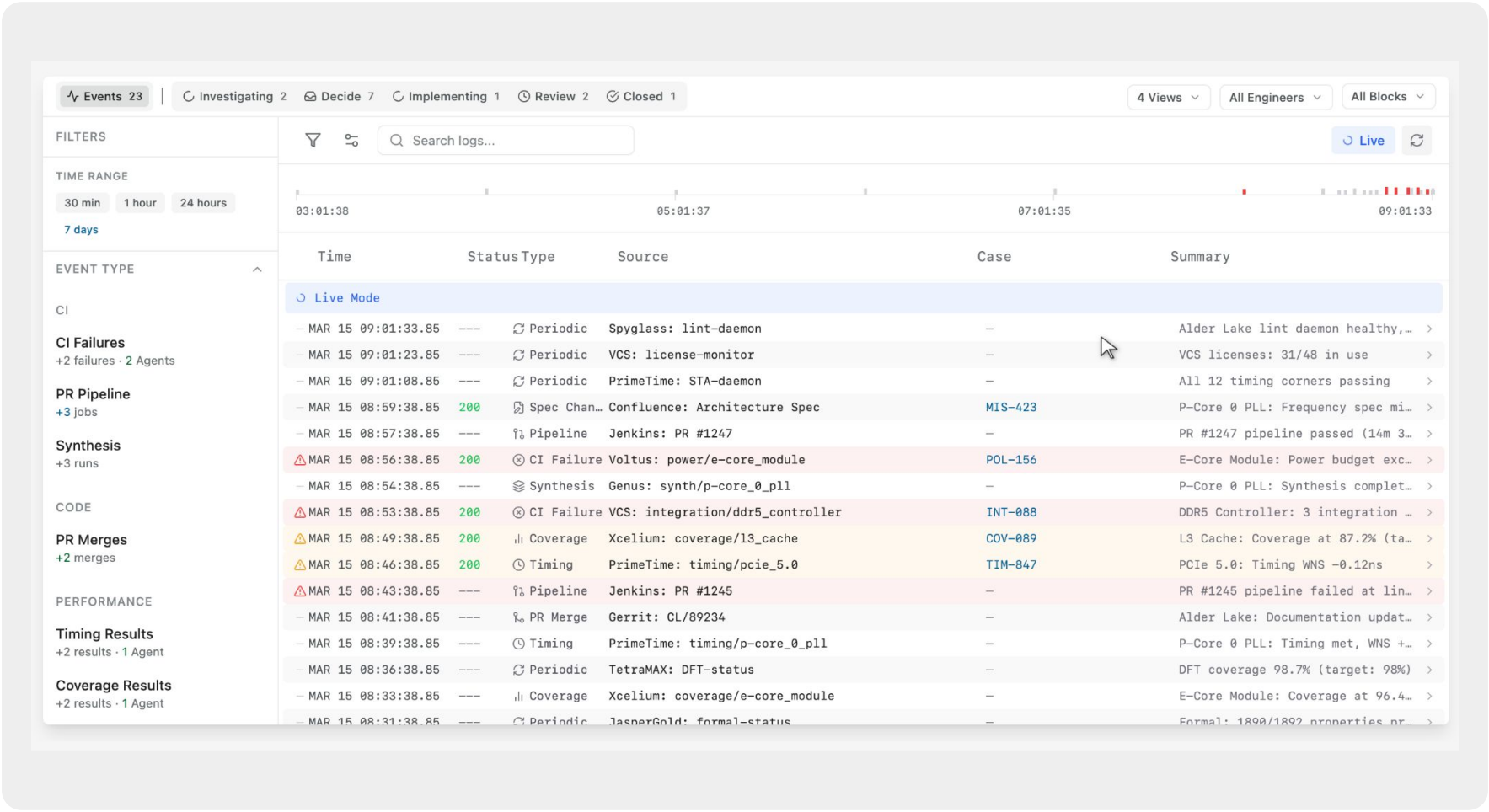
---

Custom ASICs for 6 customers

# Introducing Visibl: AI-Native Broadcom as a Service

AI speed and economics. Hardware Defensibility.


Events 23
Investigating 2
Decide 7
Implementing 1
Review 2
Closed 1
Views
All Engineers
All Blocks
Search cases...
CASES
Ring Stop Timing Violation: P... 785d
+90 · 5 Files
CLK_FREQ Mismatch: Spec 5.1... 2h
+30 · 1 File
L3 Cache MESI protocol missin... 2d
No changes
Display pipe 3 timing closure a... 16h
+45 · 4 Files
Thread Director P-Core/E-Core ... 1d
+45 · 4 Files
TIM-847
Reactive · CI FAILURE
Ring Stop Timing Violation: P-Core 0 → L3 Slice 3 Path
INTERCONNECT · Unknown ·
Ran 10 Explore agents
Root Cause Identified
PR #734 optimized ring stop arbitration from 3-cycle to 2-cycle, but was only verified at TT corner. SS corner shows -15ps setup violation on...
FIX OPTIONS
1–4 select · ↑↓ navigate
1 Update mc_ch0_arb to match spec Recommended
Modify RTL implementation to conform to specification
Refine ⌘⌫ (optional)
Run ⌘↵
2 Update spec to match RTL
Revise specification to reflect current implementation
3 Request design waiver
Document deviation and request formal approval
4 Describe your own approach...
Memory Controller 1 case
REG-201 Executing
DDR5 read latency increased by 2ns after PHY update
Drill into block
↑↓ navigate · Enter select · Esc close
1 Layers
ACME Pinnacle · 62 blocks · 1 affected


Events 23
Investigating 2
Decide 7
Implementing 1
Review 2
Closed 1
4 Views
All Engineers
All Blocks
FILTERS
TIME RANGE
30 min
1 hour
24 hours
7 days
EVENT TYPE
CI
CI Failures
+2 failures · 2 Agents
PR Pipeline
+3 jobs
Synthesis
+3 runs
CODE
PR Merges
+2 merges
PERFORMANCE
Timing Results
+2 results · 1 Agent
Coverage Results
+2 results · 1 Agent
Search logs...
Live
03:01:38
05:01:37
07:01:35
09:01:33
Time
Status
Type
Source
Case
Summary
Live Mode
MAR 15 09:01:33.85 --- Periodic Spyglass: lint-daemon – Alder Lake lint daemon healthy,…
MAR 15 09:01:23.85 --- Periodic VCS: license-monitor – VCS licenses: 31/48 in use
MAR 15 09:01:08.85 --- Periodic PrimeTime: STA-daemon – All 12 timing corners passing
MAR 15 08:59:38.85 200 Spec Chan… Confluence: Architecture Spec MIS-423 P-Core 0 PLL: Frequency spec mi…
MAR 15 08:57:38.85 --- Pipeline Jenkins: PR #1247 – PR #1247 pipeline passed (14m 3…
MAR 15 08:56:38.85 200 CI Failure Voltus: power/e-core_module POL-156 E-Core Module: Power budget exc…
MAR 15 08:54:38.85 --- Synthesis Genus: synth/p-core_0_pll – P-Core 0 PLL: Synthesis complet…
MAR 15 08:53:38.85 200 CI Failure VCS: integration/ddr5_controller INT-088 DDR5 Controller: 3 integration …
MAR 15 08:49:38.85 200 Coverage Xcelium: coverage/l3_cache COV-089 L3 Cache: Coverage at 87.2% (ta…
MAR 15 08:46:38.85 200 Timing PrimeTime: timing/pcie_5.0 TIM-847 PCIe 5.0: Timing WNS −0.12ns
MAR 15 08:43:38.85 --- Pipeline Jenkins: PR #1245 – PR #1245 pipeline failed at lin…
MAR 15 08:41:38.85 --- PR Merge Gerrit: CL/89234 – Alder Lake: Documentation updat…
MAR 15 08:39:38.85 --- Timing PrimeTime: timing/p-core_0_pll – P-Core 0 PLL: Timing met, WNS +…
MAR 15 08:36:38.85 --- Periodic TetraMAX: DFT-status – DFT coverage 98.7% (target: 98%)
MAR 15 08:33:38.85 --- Coverage Xcelium: coverage/e-core_module – E-Core Module: Coverage at 96.4…
MAR 15 08:31:38.85 --- Periodic JasperGold: formal-status – Formal: 1890/1892 properties pr…

## Value Proposition

1. **Schedule** – ~4x NRE Time
2. **Cost** – 20-30x NRE (Non-Recurring Engineering Cost) Improvement
3. **Access** – No chip team required

Neuralink - 5 mo. span

First ever partner to leverage AI systems in chip design, weekly meetings

Start of YC - Talk with more companies

Discover bespoke nature of toolchain - does not scale well, requires FDE

Pivot to design-as-a-service - 1 mo. ago

AI-Native Broadcom


BTQ

“Many chips, like those used in embedded systems, are in mature technologies we could manufacture in the United States.

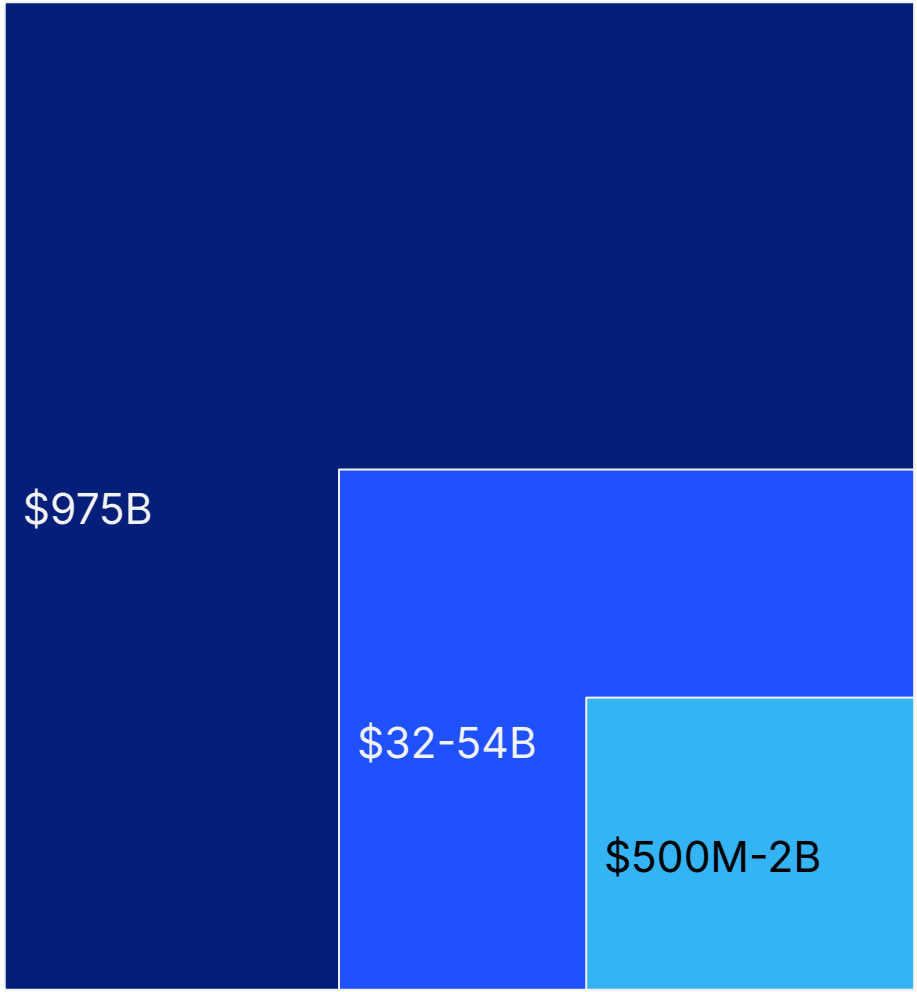
It’s disappointing how slow it is to put into production in 2026.

If Visibl can reduce the time it takes to go from idea to tape out, even by a few months, it would save even small companies like BTQ Technologies 6 or 7 figures over time.”

*- Sean Hackett - Head of Silicon Product @ BTQ*

## General Chip + FPGA → ASIC

Eliminate High NRE Cost, improve margins, open entire long-tail market. A new category of design house designed for maximum throughput of ASICs.




All figures in USD

## Series A Targets

Revenue Target: $2M

## Use of Funds

Hire SWEs & ASIC designers (chip design)

Foundry Services (MPW)

# Our Seed Round

Appendix - Mostly Redacted
[Contact if interested]

founders @visiblsemi.com

APPENDIX

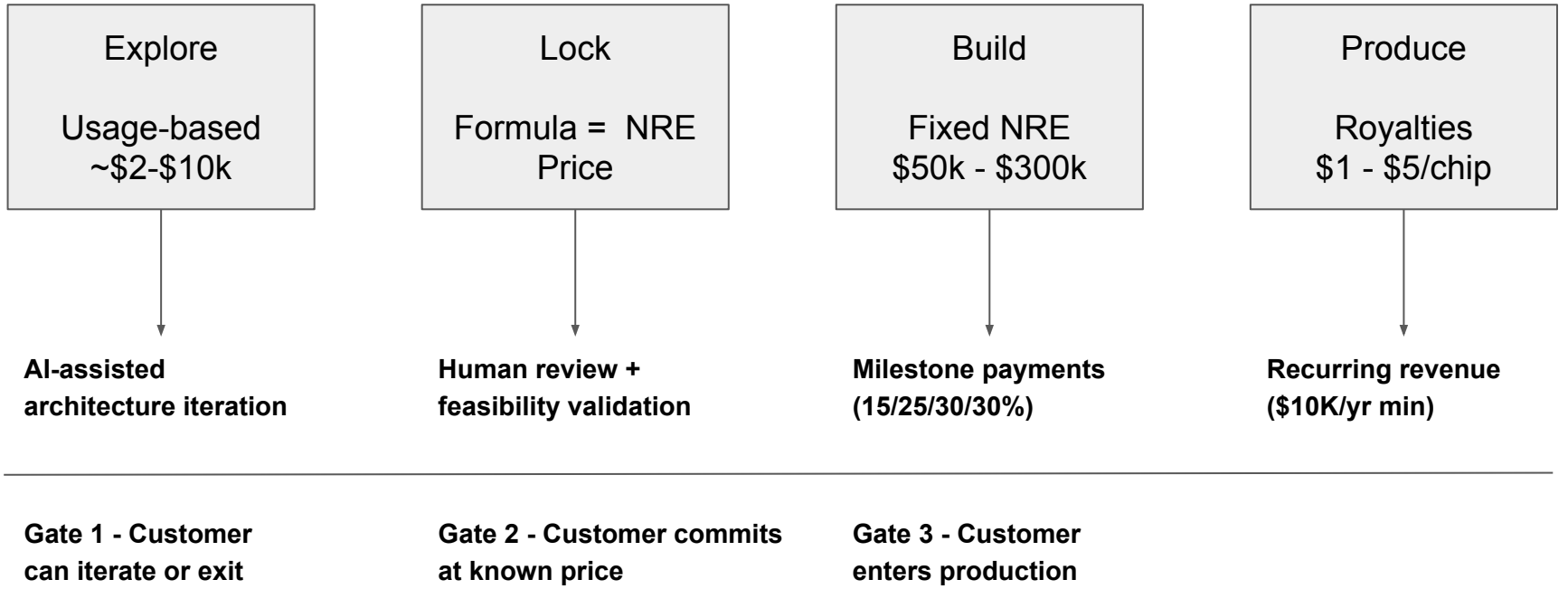
# Broadcom's Revenue Model: What We Are Replicating

| Aspect | Broadcom | Traditional Design House | Visibl |
|---|---|---|---|
| **Pricing Model** | Multi-year strategic partnership | High NRE upfront | **Explore → Lock → Build** |
| **Design Fee** | Embedded in system price | $3-50M explicit NRE | Usage-based → Formula-based NRE |
| **Key Metric** | Gigawatts / XPU clusters | Engineering hours | **Architecture parameters** |
| **Minimum Deal** | $1B+ (smallest observed) | $1-10M | **Pay-as-you-go to start** |
| **Customer Risk** | Low (Broadcom absorbs) | High (pay before knowing) | **Low (price set at arch lock)** |
| **Barrier to Entry** | Impossible for 99% | High | **Low + transparent formula** |

*CNBC - Hock Tan $100B Forecast* | *TrendForce - Anthropic $21B Orders* | *Futurum Group - Broadcom Q4 FY2025 Earnings*

# AWS-Like Configurator: Architecture Determines Cost

Our Model: Staged Pricing Based on Measurable Architecture



| Node | Wafer Cost | Mask Set | MPW Cost |
|---|---|---|---|
| **180nm** | $800-1,500 | $200K-400K | $15K-25K |
| **130nm** | $1,000-1,800 | $400K-800K | $20K-30K |
| **90nm** | $1,800-2,200 | $800K-1.2M | $25K-40K |
| **65nm** | $2,000-2,600 | $1.3M-2M | $45K-70K |
| **40nm** | $2,400-3,000 | $2M-3M | $60K-90K |
| **28nm** | $2,550-3,450 | $3M-5M | $70K-130K |
| 22nm | $3,000-4,000 | $4M-6M | $100K-150K |
| 14/16nm | $3,800-5,200 | $5M-8M | $150K-250K |
| 7nm | $8,100-10,900 | $10M-15M | $200K-400K |
| 5nm | $16,000-21,300 | $12M-18M | $300K-500K |
| 3nm | $17,000-22,000 | $15M-40M | $400K-700K |

# Strategic Customer Examples

One real proof point + three strategic market examples

## BTQ Technologies

Real Proof Point

### Direct Replacement / Secure Coprocessor

*Problem:* *Mature-node chip programs are too slow and expensive*

*Visibl Value:* *Faster path to first silicon, less engineering overhead*

*Expected Gain:* *Months faster, 6-7 figure program savings*

## Flock Safety

Strategic Example

### Companion ASIC

*Problem:* *Module-based hardware inefficient for always-on edge sensing*

*Visibl Value:* *Custom ALPR / audio / preprocessing silicon*

*Expected Gain:* *2-5x lower always-on power, 20-40% lower BOM*

## Verkada

Strategic Example

### Companion ASIC

*Problem:* *Edge AI camera economics constrained by merchant compute*

*Visibl Value:* *Custom vision companion silicon*

*Expected Gain:* *2-4x better perf/watt, 15-35% lower BOM*

## BRINC

Strategic Example

### Companion ASIC

*Problem:* *Drone mission electronics spread across too many parts*

*Visibl Value:* *Consolidate mission compute/control into custom silicon*

*Expected Gain:* *20-40% lower board footprint, 15-30% lower BOM*

# BTQ Technologies

Real Proof Point

## Visibl Integration Mode: Direct Replacement / Secure Coprocessor

### Customer Pain

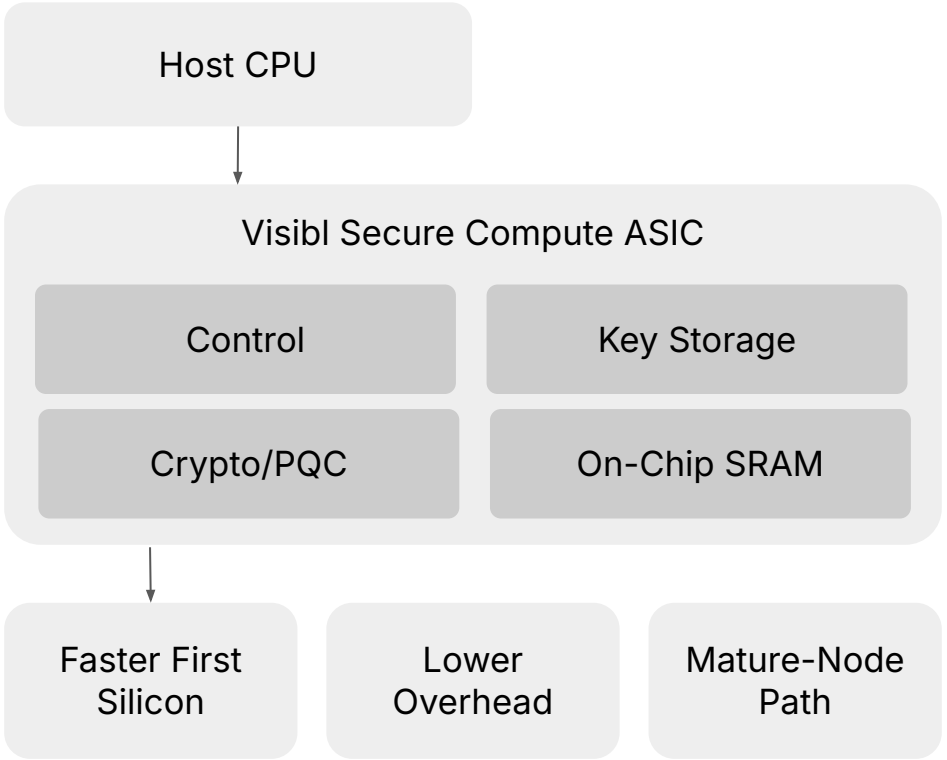
- ➔ Implementation effort and DV burden
- ➔ Layout and bringup complexity
- ➔ Manufacturing-partner coordination
- ➔ Silicon engineers tied up for full cycle

### What Visibl Delivers

- ➔ Faster time-to-first-silicon
- ➔ Lower engineering overhead
- ➔ Economically viable mature-node execution
- ➔ Practical path to purpose-built secure-compute ASIC

### Expected Gains

- ➔ Time: Months faster to first silicion
- ➔ Cost: 6-7 figure program cost savings
- ➔ Staffing: Reduced in-house chip team needs




*"If Visibl can reduce the time from idea to tape out, even by a few months, it would save companies like BTQ 6-7 figures."* **- Sean Hackett, Head of Silicon Product @ BTQ**

APPENDIX

# Flock Safety

Strategic Example

## Visibl Integration Mode: Companion ASIC for Edge Sensing

### Why Flock Matters

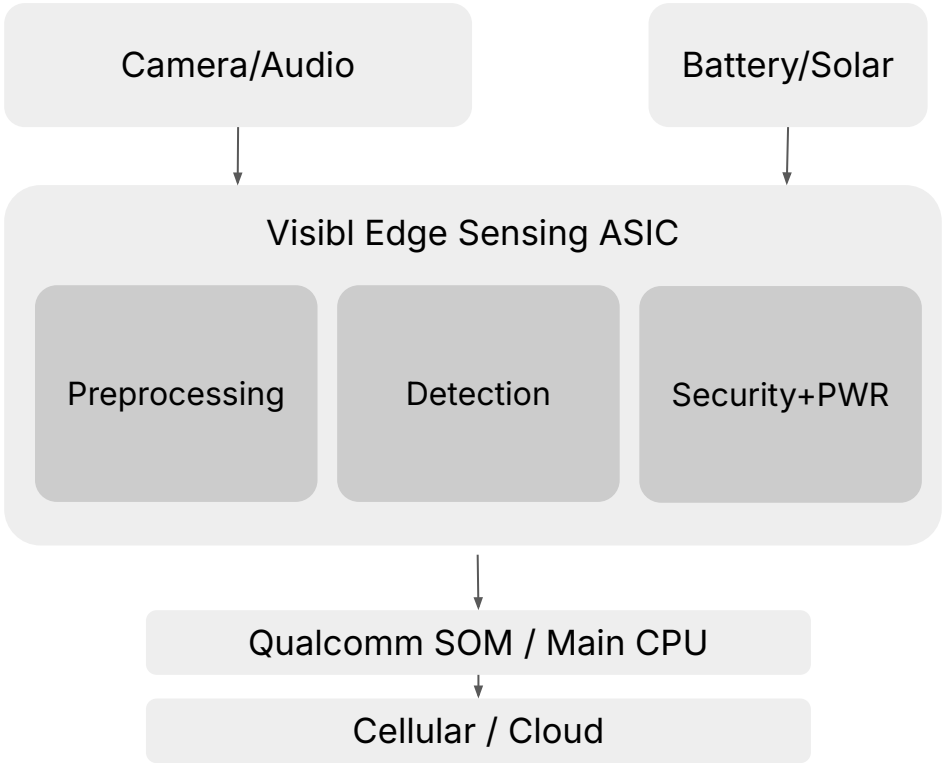
- ➔ Solar-powered, infrastructure-free ALPR devices
- ➔ Built on Lantronix Open-Q 624A SOM (Qualcomm 624)
- ➔ Clearest public example of prototype-to-production path

### Customer Pain

- ➔ Always-on sensing needs low power
- ➔ Solar/battery constraints at scale
- ➔ Merchant SOM has excess capability/overhead

### What Visibl Would Build

- ➔ Image preprocessing + ALPR pipeline
- ➔ Audio event detection
- ➔ Compression/filtering + low-power wake
- ➔ Security and local policy logic




*2-5x lower power | 2-4x better perf/watt | 20-40% lower BOM | 30-70% less bandwidth (less cloud data)*

APPENDIX

# Verkada

Strategic Example

## Visibl Integration Mode: Companion ASIC

### Why Verkada Matters

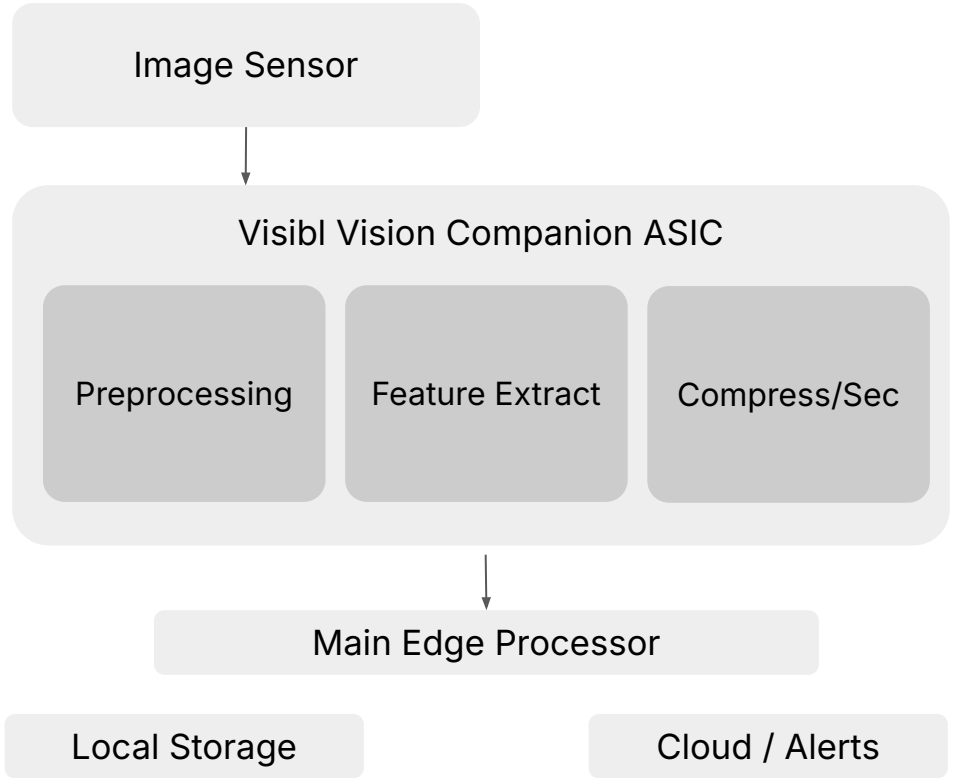
- ➔ Onboard AI-powered search and alerts
- ➔ Real-time edge analytics + built-in storage
- ➔ Camera-first architecture (not legacy NVR)

### Customer Pain

- ➔ Once edge analytics are core, economics depend on hardware
- ➔ Power envelope and thermal limits matter
- ➔ Merchant compute often overbuilt at scale

### What Visibl Would Build

- ➔ Image preprocessing + feature extraction
- ➔ Compression + local analytics
- ➔ Encryption/security + storage orchestration
- ➔ Event filtering for cloud upload




*2-4x better perf/watt | 15-35% lower BOM | 30-70% less storage/bandwidth*

# BRINC

Strategic Example

## Visibl Integration Mode: Companion ASIC for Mission Electronics

### Why BRINC Matters

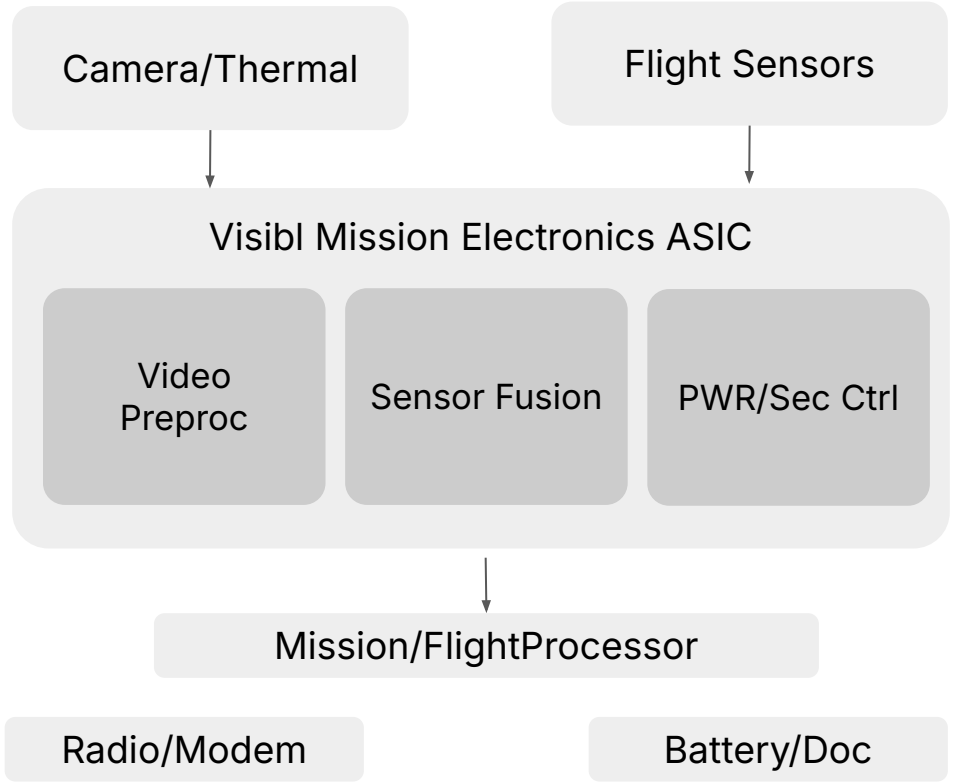
- ➔ Public-safety drones with thermal + visible imaging
- ➔ Long endurance + multiple connectivity paths
- ➔ Docking/charging workflows + secure remote ops

### Customer Pain

- ➔ Too many critical functions across too many chips
- ➔ Power, heat, reliability, cost, supply chain complexity
- ➔ Custom silicon = real moat for endurance + differentiation

### What Visibl Would Build

- ➔ Video preprocessing + sensor fusion
- ➔ Connectivity orchestration
- ➔ Security / mission control
- ➔ Battery / dock / payload management




*20-40% lower board area | 20-50% lower power | 15-30% lower BOM | Better endurance*

APPENDIX

## BTQ Technologies

Proves: Commercial interest

Customers care about compressing the path from idea to tapeout. Mature-node economics matter now.

## Flock Safety

Proves: Migration path exists

Merchant SOMs are used to get to market fast. Natural migration path to production silicon when power/battery economics matter.

## Verkada

Proves: Edge AI = hardware margin

Onboard analytics create hardware margin pressure. Custom silicon improves product economics without frontier nodes.

## BRINC

Proves: BOM collapse matters

Board-level integration matters. Edge platforms gain from custom silicon even when the workload is not AI training.

End