LAB 91

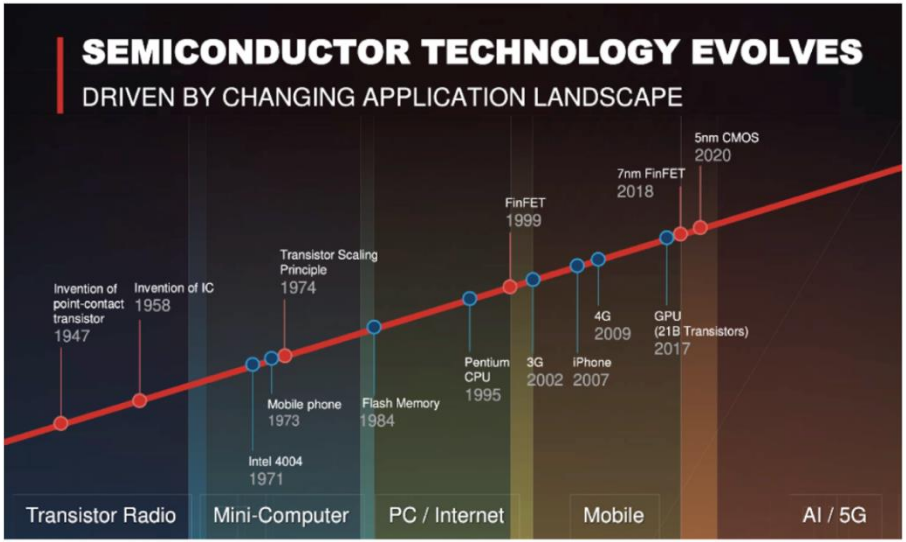
The Next Great American Chip Manufacturing Company

April 2026

THE $ 1 TRILLION PROBLEM

Silicon is running out of atoms to shrink.

After 60 years of Moore's Law, the industry faces a hard physical wall. Transistors are now just a handful of atoms wide — and traditional materials cannot go further.



Transistor Leakage

At sub-3nm, quantum tunneling causes catastrophic power leakage in silicon FETs. Performance gains stall.

RF Switch Ceiling

Silicon/SOI RF switches, critical components in comms chains, are maxed at 60–80 fs Ron*Coff [FoM]— they don’t scale to higher 5G/6G frequencies

Memory Wall

SRAM density has hit 38 Mb/mm² at TSMC N2 with no scaling path. HBM supply is constrained. AI workloads are memory-starved.

WHY 2D MATERIALS ARE INEVITABLE

MoS_2 is already on the roadmaps of TSMC, Intel, and Samsung — not as a research project, but as the required path to sub-1nm

Thickness:
0.65 nm — truly 2D, zero bulk leakage

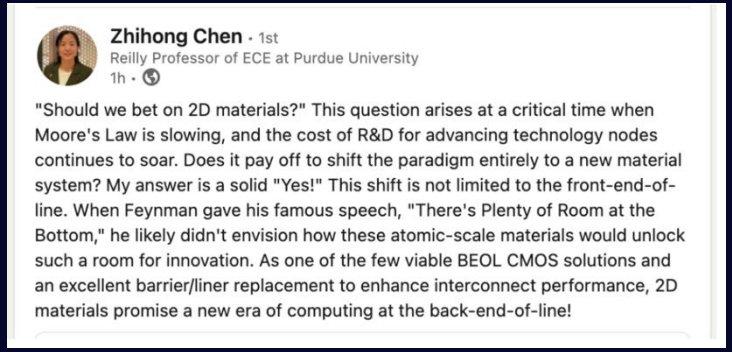
Tunable Bandgap:
1.8 eV direct bandgap — ideal for logic, RF, and memory

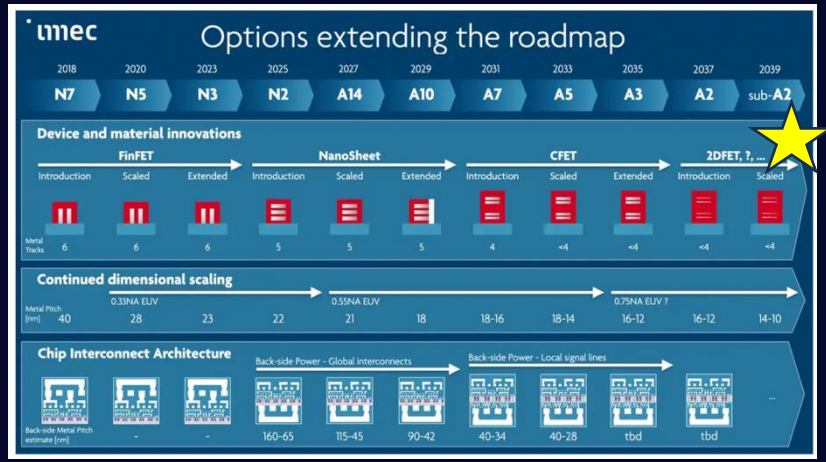
Mobility:
Electron mobility competitive with Si at atomic scale

Radiation hardness:
No bulk oxide trap sites — intrinsic rad tolerance

BEOL-compatible:
ALD deposition at low temp — integrates on existing nodes

2D adoption is not IF. It's WHEN — and Lab 91 is already building production-ready devices.





FIRST MOVER ADVANTAGE — HOW WE BEAT THE FIELD

The 2D materials space has many pretenders. Lab 91 has a structurally different — and superior — approach.

Category	MOCVD Players (PhantaField, CDimension, FS2, Nexstrom, Aixtron)	Lab 91 (ALD-First)	Why It Matters
Process	MOCVD on academic grade tools, which is not reproducible on production grade tools. Often high temp (~ 1000 °C)	ALD <400 °C → Full BEOL integration	Lab 91 devices can integrate directly onto existing chips.
Yield	Layer transfer kills yield; high defect density	Atomically precise; conformal growth	Production-viable yield from day 1. The rest are still in research mode.
Node strategy	Chasing leading edge (< 1nm); Far higher degree of difficulty (N & P type contacts, EUV patterning etc)	Old nodes, new material introduction at the back-end; Keeps old fab lifecycle going	Revenue NOW on 130–22nm nodes. No $20B fab required.
IP	Process-focused; limited device IP – “Build it, they will come” approach	Device IP + process IP + EDA software stack	Layered moat: patent, process know-how, and proprietary device IP/ EDA tools.
Competitive Advantage	Undifferentiated offerings from various academic spinouts (UC SB, MIT, NUS)	First mover in ALD with two best-in-class devices (RF and memory)	Process selection matters; Lab 91 is following a commercially scalable pathway with clear market validation

4 MEGATRENDS — TAILWINDS FOR LAB 91

01

Earth → Space

Orbital compute is exploding

SpaceX, Amazon LEO, and many other players are deploying satellite constellations that demand ultra-low-power, radiation-hard RF switches. Silicon cannot survive orbit. Our MoS_2 switch is the only sub-10 fs option with intrinsic rad-tolerance.

02

5G → 6G

For a Low latency, hyper connected future

5G/6G front-ends must operate up to V-band and W-band (60–300 GHz). GF's 9SW SOI tops out at 60 fs Ron·Coff and 60 GHz. Our switch operates X-band to 480 GHz at 7 fs — a 10× performance leap.

03

Compute → Memory

Breaking through the memory wall

SRAM is stuck at 38 Mb/mm² (TSMC N2). HBM is supply-constrained. AI inference is bottlenecked. Our MoS_2 memristor enables monolithic 3D memory stacked directly on logic — breaking the wall.

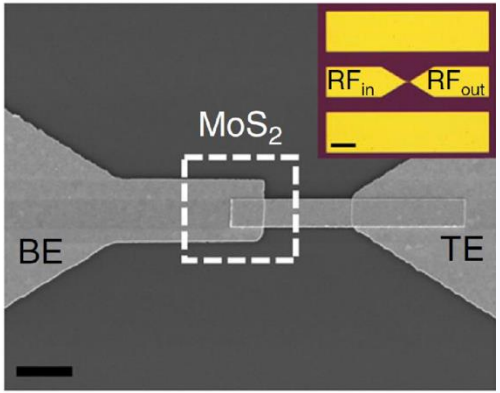
04

ALD-W → ALD-Mo

A favorable supply chain trend

ALD Molybdenum is replacing Tungsten as the leading interconnect metallization. This trend funds our process R&D — the same precursors and tools we use for MoS_2. ASM is our ideal partner.

PRODUCT 1: MoS_2 RF SWITCH FOR NEXT GEN COMMS



Ron·Coff: **7 fs**	*vs 60–80 fs best GF 9SW SOI (10× better)*
Switching speed: **500 ps**	*vs 10–100 ns incumbent (200× faster)*
Static power: **0 mW**	*No DC bias — zero idle dissipation*
Bandwidth: **X → 480 GHz**	*Ka/V/W-band native; no performance cliff*
Architecture: **Stackable**	*Cascade units to any power level*

Why These Markets MUST Have Our Switch

Satellite / Space Comms

Phased-array beamforming for LEO constellations requires sub-ns switching at Ka/V-band. Radiation hardness is non-negotiable. GaAs/SOI fail on both counts. No other switch exists.

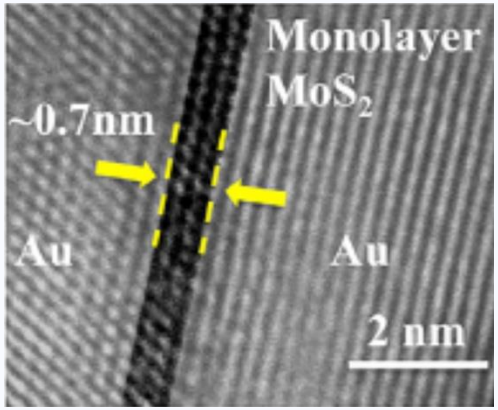
5G/6G Mobile Front-End

6G front-ends need switches up to V/W-band. The entire incumbent RF SOI roadmap tops out at 60 GHz — our switch natively covers the full 6G spectrum at 10× better Ron·Coff.

AI Edge / IoT / Robotics

Always-on devices require zero static power. Our switch draws nothing at idle, enabling true zero-power standby — the only RF switch architecture that scales to 1T IoT devices.

PRODUCT 2: MoS_2 MEMRISTOR — BREAKING THE AI MEMORY WALL



Lab 91's Monolayer MoS_2 Cell — 0.65 nm

Thickness: 0.65 nm	*Single monolayer — enables true 3D stacking on logic*
Standby power: 0 pJ/bit	*Non-volatile — no refresh, no idle leakage*
Write energy: 50 pJ	*vs 1–10 nJ for DRAM write — 20–200× more efficient*
Switching speed: <1 ns	*Sub-nanosecond — DRAM-class latency, NVM reliability*
Radiation: Intrinsic	*No bulk oxide trap sites — zero rad-hard process premium*

Why These Markets MUST Have Our Memristor

AI Accelerator (SRAM Wall)

TSMC N2 SRAM is maxed at 38 Mb/mm². Our 3D-stackable memristor breaks this ceiling — enabling 10× more on-chip memory without area penalty.

3D DRAM / HBM Alternative

HBM is supply chain-constrained. Our atomically thin memristor allows 3D stacking at the back end, directly on top of compute/logic dies

Space / Defense Computing

Orbital data centers need non-volatile, rad-hard memory for AI inference in-orbit. DRAM fails from radiation; NOR flash is too slow. Our memristor solves both with zero idle power.

MARKET OPPORTUNITY — MULTIPLE MULTI-BILLION PATHS

RF Switch Market

TAM $28B
by 2030

SAM $4.2B
Space + 5G/6G

SOM $420M
Year 5 target

Key segments:

- Satellite LEO constellations
- 5G/6G smartphone front-ends
- Defense AESA radar systems
- Edge AI / IoT always-on devices

Advanced Memory Market

TAM $180B
by 2030

SAM $18B
AI accelerator + space

SOM $1.8B
Year 6 target

Key segments:

- AI accelerator on-chip SRAM augmentation
- 3D DRAM (HBM alternative)
- Orbital data center non-volatile storage
- Defense rad-hard computing modules

BUSINESS MODEL & IP MOAT — HIGH-MARGIN, DEFENSIBLE

Fabless chip company. We own the IP, process flows, and EDA software. Fabs manufacture — we capture the margin.

Chip Sales

High-margin MoS_2 RF Switch and Memristor chips sold to systems integrators, satellite OEMs, and AI accelerator chip OEMs. Recurring revenue per wafer. Move to fully integrated modules and other device categories over time (mixed RF/Photonics)

NRE Contracts

Non-Recurring Engineering fees from customers requiring custom device development. We are working on landing a $15M contract from DoD-funded satellite operator.

Process IP Licensing

License proprietary ALD process flows and Best Known Methods (BKMs) to equipment makers and foundries integrating 2D into their nodes.

EDA Software / Models

Proprietary device models, SPICE parameters, and EDA toolkits bundled with chips. Software creates switching costs and recurring license revenue.

WE ARE RAISING A $5M SEED — MILESTONES & USE OF PROCEEDS

Use of Proceeds

- 40% Process Engineering & ALD
- 25% Personnel (Full time engineering staff – 3 to 4 key hires will be made, including a full time CTO)
- 20% Device Integration & Testing
- 15% EDA Software licenses, IP & Legal, Office/Lab space

ASM

Our ALD equipment partner, ASM, the world leader in ALD technologies

Key Milestones (18–24 months)

Stabilize ALD Process on major ALD equipment vendor platform

Establish BKM with ASM. Achieve repeatable MoS_2 on 8" / 12" wafers.

EDA Tool Development: Correlate Process → Device

Build physics-based model ("digital twin") linking ALD params to device parameters (ex: Ron·Coff). This is our EDA foundation for device design rules and metrology.

RF Switch Design Win

Qualify MoS_2 RF switch chip with satellite OEMs for Ka-band beamforming. Initial parts can be discrete / in package (SP4T). First commercial revenue.

Memristor Development

Demonstrate stackability and endurance of memristor for high density SRAM/3D DRAM

DOE Genesis Award

Close DOE Genesis Phase II grant with UNM/LANL/UMD consortium. Milestone funding to accelerate Series A path. Target: 2027

Series A Ready

Two products in qualification, target raise: $25–35 M.

OUR TEAM - BUILT TO WIN IN THE CUTTHROAT SEMI INDUSTRY

Anand Chamarthy

CEO / Co-Founder

UT Austin EE'13. A 2D materials 'lifer' since the graphene era (~ 09). Drives strategy, technical roadmap, BD, and customer relationships.

Brian Belden

COO

Ex-Freescale/Motorola executive who ran Austin MOS11/MOS13 fabs. Has driven novel films and processes from R&D into high-yield, production (worked with Lisa Su and Gregg Bartlett). Knows what it takes to scale.

Deji Akinwande

Chief Scientist / Co-Founder

UT Austin ECE Professor and globally recognized pioneer in 2D materials. Author of foundational 2D research cited by the world's biggest semi companies.

Andy Beers

Chief Process Officer

Ex-Applied Materials, AMD, and Motorola. A master of semiconductor process engineering, capital equipment, and global supply chain. Previously at OnWafer Technologies, Inc. (acq. by KLA-Tencor in 2007)

“I wonder if it isn’t time for someone to start the next great U.S. chip manufacturing company”

- Ben Thompson, Stratechery (2020)