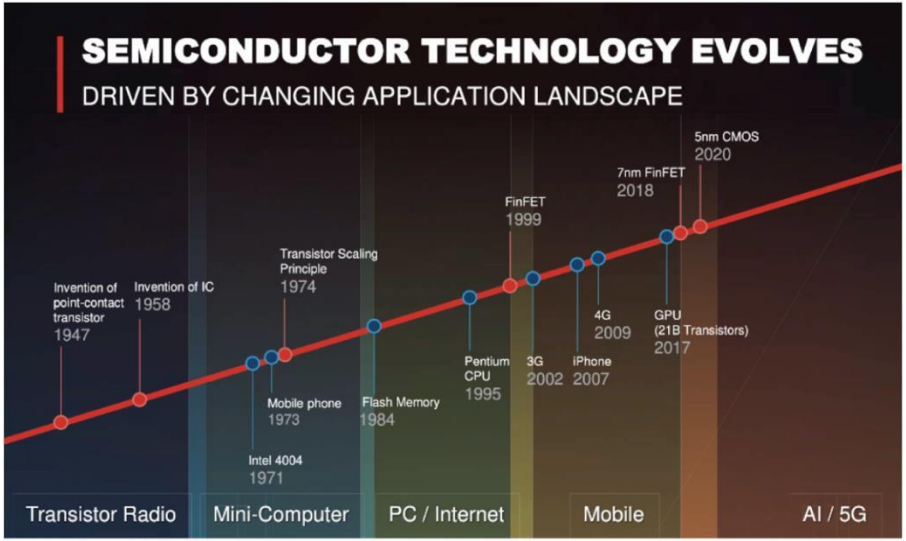
The Next Great American Chip Manufacturing Company

August 2026

THE $ 1 TRILLION PROBLEM

Silicon is running out of atoms to shrink.

After 60 years of Moore's Law, the industry faces a hard physical wall. Transistors are now just a handful of atoms wide — and traditional materials cannot go further.



Transistor Leakage

At sub-3nm, quantum tunneling causes catastrophic power leakage in silicon FETs. Performance gains stall.

RF Switch Ceiling

Silicon/SOI RF switches, critical components in comms chains, are maxed at 60–80 fs Ron*Coff [FoM]— they don’t scale to higher 5G/6G frequencies

Memory Wall

SRAM density has hit 38 Mb/mm² at TSMC N2 with no scaling path. HBM supply is constrained. AI workloads are memory-starved.

WHY 2D MATERIALS ARE INEVITABLE

MoS_2 is already on the roadmaps of TSMC, Intel, and Samsung — not as a research project, but as the required path to sub-1nm

Thickness:
0.65 nm — truly 2D, zero bulk leakage

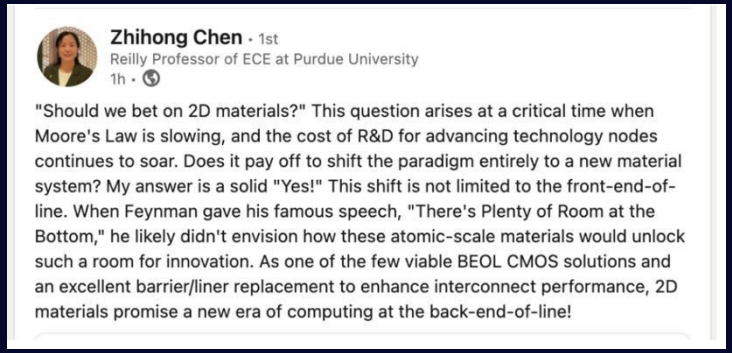
Tunable Bandgap:
1.8 eV direct bandgap — ideal for logic, RF, and memory

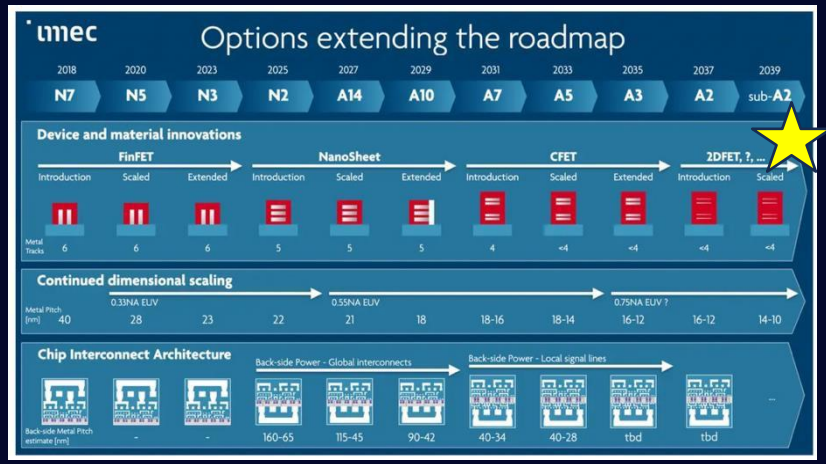
Mobility:
Electron mobility competitive with Si at atomic scale

Radiation hardness:
No bulk oxide trap sites — intrinsic rad tolerance

BEOL-compatible:
ALD deposition at low temp — integrates on existing nodes

2D adoption is not IF. It's WHEN — and Lab 91 is already building production-ready devices.





FIRST MOVER ADVANTAGE — HOW WE BEAT THE FIELD

The 2D materials space has many pretenders. Lab 91 has a structurally different — and superior — approach.

Category	MOCVD Players (PhantaField, CDimension, FS2, TDS Inno, Nexstrom, Yuanjiwei)	Lab 91 (ALD-First)	Why It Matters
Process	MOCVD on academic grade tools, which is not reproducible on production grade tools. Often high temp (~ 1000°C)	ALD <400°C → Full BEOL integration	Lab 91 devices can integrate directly onto existing chips.
Yield	Layer transfer kills yield; high defect density	Atomically precise; conformal growth	Production-viable yield from day 1. The rest are still in research mode.
Node strategy	Chasing leading edge (< 1nm); Far higher degree of difficulty (N & P type contacts, EUV patterning etc)	Old nodes, new material introduction at the back-end; Keeps old fab lifecycle going	Revenue NOW on 180–12nm nodes. No $20B fab required.
IP	Process-focused; limited device IP – "Build it, they will come" approach	Device IP + process IP + EDA software stack	Layered moat: patent, process know-how, and proprietary device IP/ EDA tools.
Competitive Advantage	Undifferentiated offerings from various academic spinouts (UC SB, MIT, NUS)	First mover in ALD with a best-in-class device perfectly timed for RF and CPO	Process selection matters; Lab 91 is following a commercially scalable pathway with clear market validation

4 MEGATRENDS — TAILWINDS FOR LAB 91

01

Earth → Space

Orbital compute is exploding

SpaceX Starlink, Amazon LEO, Starcloud and others are deploying constellations that demand ultra-low-power, radiation-hard RF switches for satellite to ground terminal comms. Our MoS_2 RF switch is the only wideband, sub-10 fs option with intrinsic rad-tolerance.

02

1.6 Tbps -> 3.2 Tbps

All AI data center links will be optical within 5 years

Data Center build-outs are stalling/becoming increasingly political. As a result, there is a push to maximize productivity in existing data centers (Tokens/Second + Tokens/Watt). Hyperscalers and frontier labs are increasingly demanding 3.2 Tbps optical interconnects on 400G lanes

03

5G -> 6G

For an increasingly connected future

5G/6G front-ends for smartphones, AR/VR, edge and physical AI must operate up to V-band and W-band (60–300 GHz). GF's 9SW SOI tops out at 60 fs Ron·Coff and 60 GHz. Our switch operates X-band to 480 GHz at 7 fs

— a 10× performance leap

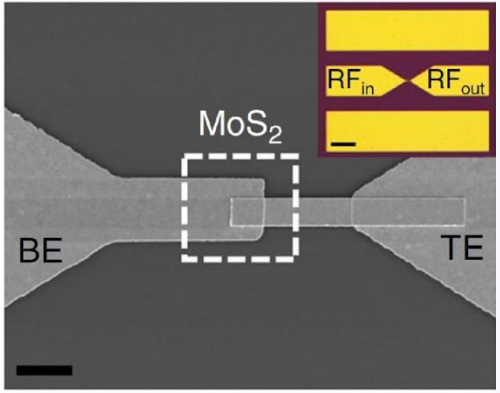
04

ALD-W → ALD-Mo

The ALD supply chain is our tailwind

ALD Molybdenum is replacing Tungsten as the leading interconnect metallization. This trend funds our process R&D — the same precursors and tools we use for MoS_2. ASM, the world leader in ALD technologies, is our ideal partner.

Our Flagship Product: MoS_2 RF SWITCH FOR NEXT WIRELESS AND CPO



Ron·Coff: **7 fs**	*vs 60–80 fs best GF 9SW SOI (10× better)*
Switching speed: **500 ps**	*vs 10–100 ns incumbent (200× faster)*
Static power: **0 mW**	*No DC bias — zero idle dissipation*
Bandwidth: **X → 480 GHz**	*Ka/V/W-band native; no performance cliff*
Architecture: **Stackable**	*Cascade units to any power level*

Why These Markets MUST Have Our Switch

3.2T AI DATACOM

Data centers need thousands of optical transceivers linking GPUs, switches, and spine fabric. As bandwidth / rack jumps 1.6T -> 3.2T, a higher speed (Thz), lower loss switch is needed for optical modulation

5G/6G Smartphone, Edge + Physical AI Front-Ends

5G/6G front-ends need switches up to V/W-band. The entire incumbent RF SOI roadmap tops out at 60 GHz — our switch natively covers the full 6G spectrum at 10× better Ron·Coff.

Satellite/Space Comms

Phased-array beamforming for LEO constellations requires sub-ns switching at Ka/V-band. Radiation hardness is non-negotiable. GaAs/SOI fail on both accounts. No other switch exists

MULTIPLE MULTI-BILLION DOLLAR PATHS

$28B

RF Switch TAM (2030)

SAM $4.2B · SOM $420M Yr 5

$31B

Photonics TAM (2036)

$20B+ MoS_2-addressable

$59B+

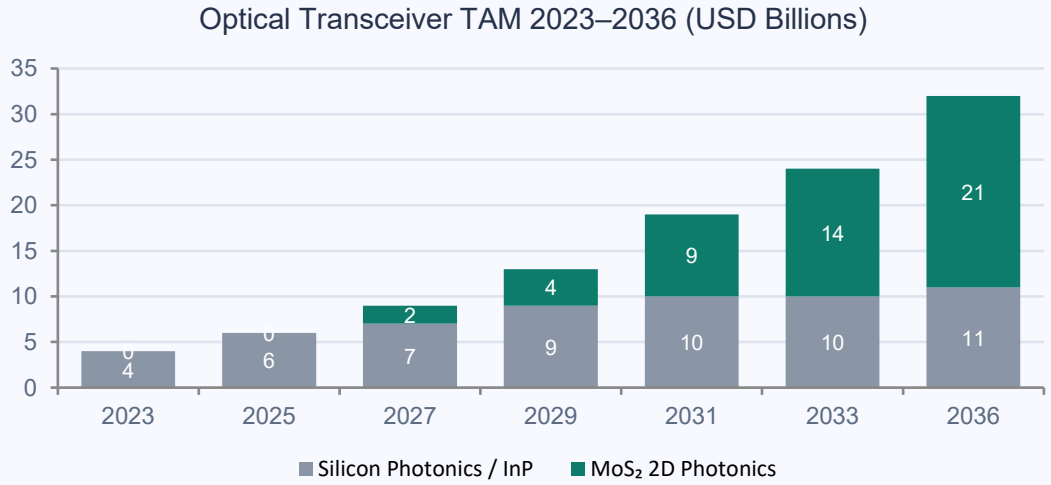
Combined Beachhead

AI DataCom + 5G/6G Telecom

2×

Market CAGR

Photonics TAM doubles 2026–2036



RF Switch Key Segments

- 3.2 Tbps CPO
- Satellite / LEO constellations
- 5G/6G smartphone front-ends
- Defense AESA radar systems
- Edge AI / IoT / robotics devices

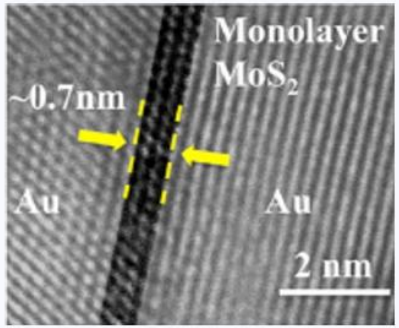
Sources: ResearchAndMarkets Jun 2026, IDC, Dell'Oro Group. MoS_2 projections assume commercial ramp from 2026.

IN THE WORKS: A MOS_2 MEMRISTOR — A FUTURE MEMORY OPTION

The same ALD process produces an atomically-thin MoS_2 memristor — a longer-dated, lower-priority option we continue to develop for 3D-stackable AI accelerator memory.

0.65 nm	0 pJ/bit	50 pJ	< 1 ns
Thickness	Standby power	Write energy	Switching speed

Potential future markets: AI accelerator on-chip SRAM augmentation, 3D DRAM / HBM alternative, and orbital non-volatile storage. These remain evaluation-stage opportunities behind our RF switch and photonic switch commercialization timeline.



Lab 91's Monolayer MoS_2 Cell — 0.65 nm

BUSINESS MODEL & IP MOAT — HIGH-MARGIN, DEFENSIBLE

Fabless chip company. We own the device IP, process flows/manufacturing know-how, and EDA software.

Chip Sales

High-margin chip/board sales sold to RF and photonics systems integrators, satellite OEMs. Recurring revenue per wafer. Our immediate goal is to win sockets / get designed in the 3.2 Tbps wave. Example end customers are Litrinium and AttoTude.

NRE/Defense Contracts

Non-Recurring Engineering fees from defense customers requiring custom device development. We are in active discussions with Leonardo-DRS (FPA group) and Lockheed Martin (MFC group)

Metrology and Process IP Licensing

Using our devices, we can measure defect density, leakage current and other critical film properties to improve process flows. This can be licensed or sold as a photomask to equipment makers and foundries integrating 2D into their nodes.

EDA Software / Models

Proprietary device models/design rules, SPICE parameters, and EDA toolkits. Proprietary layouts, contact-to-MoS2 layer spacing etc that we control with our devices

PILOT PRODUCTION LINE — TEXAS A&M & UT AUSTIN

Lab 91 is standing up its pilot ALD process line across Texas A&M University and UT Austin's Texas Institute for Electronics (TIE) — giving the company wafer-scale cleanroom access to move its devices from the lab to repeatable, production-representative runs. The effort is run in concert with a multi-university consortium — including Penn State and other partner labs — as part of the DOE Genesis program.

Texas A&M / UT Austin (TIE)

Pilot line hosts. Wafer-scale cleanroom and ALD tool access for 8”/12” MoS_2 process runs and device integration testing at the Pickle Research Campus/TIE.

Penn State & Partner Labs

Consortium members contributing complementary 2D materials growth, metrology, and device characterization expertise.

DOE Genesis Program

Milestone-based federal funding supporting the consortium's process scale-up work ahead of Lab 91's Series A raise.

Why it matters: a university-anchored pilot line de-risks process transfer before committing capital to a dedicated fab, and the multi-lab consortium structure broadens Lab 91's access to characterization equipment and 2D-materials talent beyond a single site.

WE ARE RAISING A $5M SEED — MILESTONES & USE OF PROCEEDS

Use of Proceeds

- 40% Process Engineering & ALD
- 25% Personnel (Full time engineering staff – 3 to 4 key hires will be made, including a full time CTO)
- 20% Device Integration & Testing
- 15% EDA Software licenses, IP & Legal, Office/Lab space

ASM

Our ALD equipment partner, ASM, the world leader in ALD technologies

Key Milestones (18–24 months)

Stabilize ALD Process on major ALD equipment vendor platform

Establish Best-Known-Method with ASM

EDA Tool Development: Correlate Process → Device

Build physics-based model ("digital twin") linking ALD params to device parameters (ex: Ron·Coff). This is our EDA foundation for device design rules and metrology.

Stand up 2D Pilot Line at Texas A&M

In concert with ASM and other equipment/metrology vendors

RF Switch Qualification / Design Win

Qualify MoS_2 RF switch chip 3.2 Tbps with OEMs like Litrinium and AttoTude

DOE Genesis Award

Close DOE Genesis Phase II grant with Penn State/Stephanie Law consortium. Funding to accelerate Series A path. Target: 2027

Series A Ready

RF switch in qualification, target raise: $15–25 M.

OUR TEAM - BUILT TO WIN IN THE CUTTHROAT SEMI INDUSTRY

Anand Chamarthy

CEO / Co-Founder

UT Austin EE'13. A 2D materials 'lifer' since the graphene era (~ 09). Drives strategy, technical roadmap, BD, and customer relationships.

Brian Belden

COO

Ex-Freescale/Motorola executive who ran Austin MOS11/MOS13 fabs. Has driven novel films and processes from R&D into high-yield, production (worked with Lisa Su and Gregg Bartlett). Knows what it takes to scale.

Deji Akinwande

Chief Scientist / Co-Founder

UT Austin ECE Professor and globally recognized pioneer in 2D materials. Author of foundational 2D research cited by the world's biggest chip companies.

Andy Beers

Chief Process Officer

Ex-Applied Materials, AMD, and Motorola. A master of semiconductor process engineering, capital equipment, and global supply chain. Previously at OnWafer Technologies, Inc. (acq. by KLA-Tencor in 2007)

“I wonder if it isn’t time for someone to start the next great U.S. chip manufacturing company”

- Ben Thompson, Stratechery (2020)